Operating and Service Manual

MODEL

10W1000

PART NUMBER

1002850-501

SERIAL NUMBER

8548

FORM 144 REV 1087

AMPLIFIER RESEARCH

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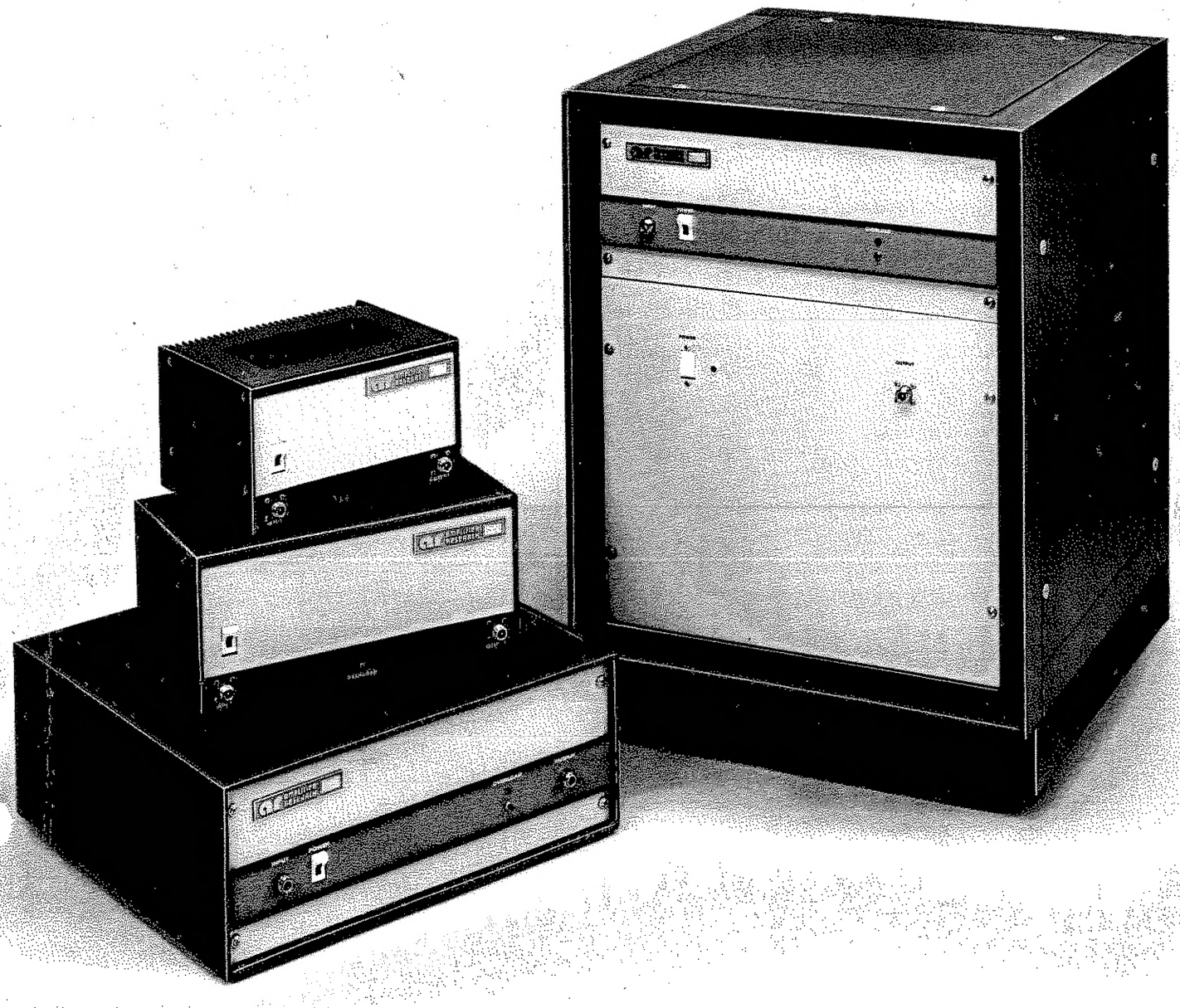
"W" Series ULTRA-BROADBAND RF POWER AMPLIFIERS



SECTION I

GENERAL INFORMATION

1.1 GENERAL DESCRIPTION

The Model 10W1000 Amplifier is a self-contained broadband unit designed for laboratory applications where instantaneous bandwidth, high gain, and moderate power output are required. Solid state technology is used exclusively to offer significant advantages in reliability and cost. A Model 10W1000 used with a frequency swept signal source will provide 10 watts of liner swept power output from 1-1000 MHz. Typical applications include antenna and component testing, wattmeter calibration, EMI Susceptibility Testing, use as a Driver for Frequency Multipliers and High Power Amplifiers, and as an RF source for Magnetic Resonance Imaging studies.

1.2 POWER SUPPLIES

This unit has a self-contained 120/240 VAC, 50/60 Hz, regulated power supply. The power consumption is a nominal 500 watts. Primary circuit fusing is provided.

1.3 SPECIFICATIONS

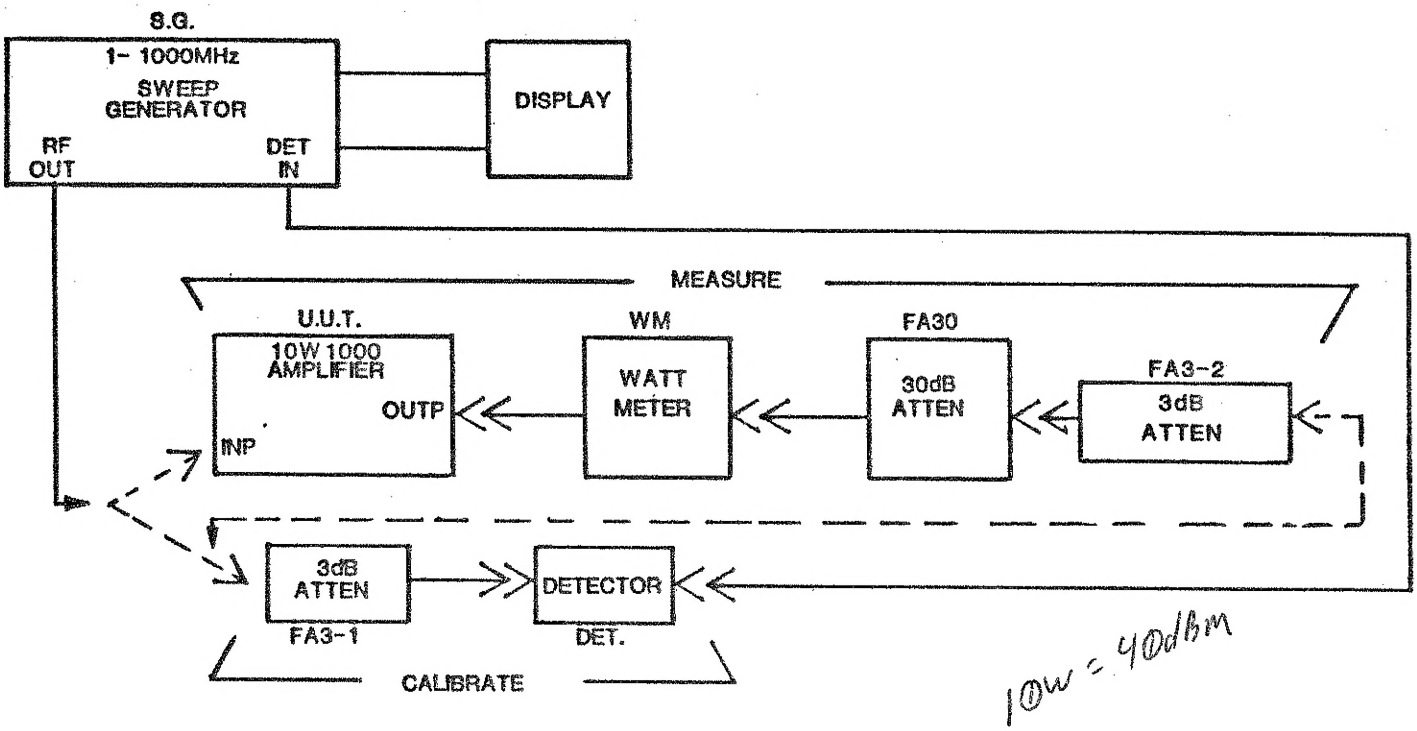
Refer to Amplifier Research Data Sheet on next page for detailed specifications.

1.4 PERFORMANCE VERIFICATION

Refer to Amplifier Research Drawing No.1001661 titled "Flatness Test Model 10W1000", located after specifications.

FLATNESS TEST
MODEL 10W1000

AMPLIFIER RESEARCH



RECOMMENDED TEST EQUIPMENT

S.G. = Sweep Generator Texscan Model VS60B or equal.
Display = Texscan Model DU120 or equal.
FA30 = Fixed attenuator 30 ±0.75 dB, 20w, Narda Model 776-30 or equal.
(2)FA3-1,2 = Fixed attenuator 3dB Texscan Model FP-50 or equal.
Det. = Detector 1-1000 MHz Texscan Model CD-50 or equal.
WM = Wattmeter Bird Model 43 w/10 watt plug, Model 10E.

The amplifier flatness shall be measured at approximately 4 watts output. (36dBm) Calibrate the test set-up as follows:

1. Adjust S.G. to produce 1-1000 MHz @ 0dBm by connecting the RF output to the detector input. Include cables, adapters, etc. that will be used to test the amplifier so all sources of error are included. Mark a line over the trace on the display - this is the 0dBm reference.
2. Add FA3-1 between the S.G. RF output and the Detector input. Mark a line over this trace to establish -3dBm reference.
3. Connect the RF output of S.G. to the input of the 10W1000. Connect FA3-1 to FA3-2 and turn the amplifier on. Adjust the RF output level of S.G. for average response between the two lines on the display that were marked previously.
4. Observe response to determine flatness tolerance of ±1.5 dB.

1001661
REV0582

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SECTION II

OPERATING INSTRUCTIONS

2.1 GENERAL

Operation of the Model 10W1000 broadband amplifier is quite simple. The input signal, whether swept or fixed in frequency, is fed into the jack marked INPUT and the amplifier output signal is taken from the jack labeled OUTPUT. The unit is turned ON by activating the power switch. In the event of a unit malfunction, protection is provided by fusing located at the rear of the unit. A polarized, three (3) wire AC power cord is also included with the unit to provide cabinet and chassis grounding to the power mains.

> CAUTION:
> THE MODEL 10W1000 AMPLIFIER IS NOT CRITICAL IN REGARDS TO SOURCE AND LOAD VSWR AND WILL REMAIN UNCONDITIONALLY STABLE WITH ANY MAGNITUDE AND PHASE OF SOURCE AND LOAD VSWR. IT ALSO HAS BEEN DESIGNED TO WITHSTAND, WITHOUT DAMAGE, RF INPUT POWER UP TO TWENTY (20) TIMES ITS RATED INPUT OF 1mW: HOWEVER, SIGNAL LEVELS HIGHER THAN 20 mW OR TRANSIENTS WITH HIGH PEAK VOLTAGES CAN DAMAGE THE AMPLIFIER. ALSO, ACCIDENTAL CONNECTION OF THE 10W1000 OUTPUT TO THE INPUT CAUSES OSCILLATIONS WHICH WILL PERMANENTLY DAMAGE THE INPUT TRANSISTOR. INTERNAL CROWBAR PROTECTION IS DESIGNED INTO THE AMPLIFIER TO PROTECT AGAINST INPUT OVERDRIVE.

The amplifier is protected by a fast acting Crowbar circuit. The Crowbar may be activated by an input signal greater than required for full output power. When the input signal reaches a level that may cause damage to the amplifier power stages, the 28 volt power supply is turned OFF and the red Overload light on the panel is activated. Typically, the input level required to activate the Crowbar is approximately +2 to +3 dBm.

To reset the Crowbar, reduce the input RF to 0dBm or lower, and push the Reset switch (S3) located by the Overload light on the front panel.

2.2 AMPLIFIER OPERATION

Figure 2.1 shows the Model 10W1000 Amplifier in pictorial form.

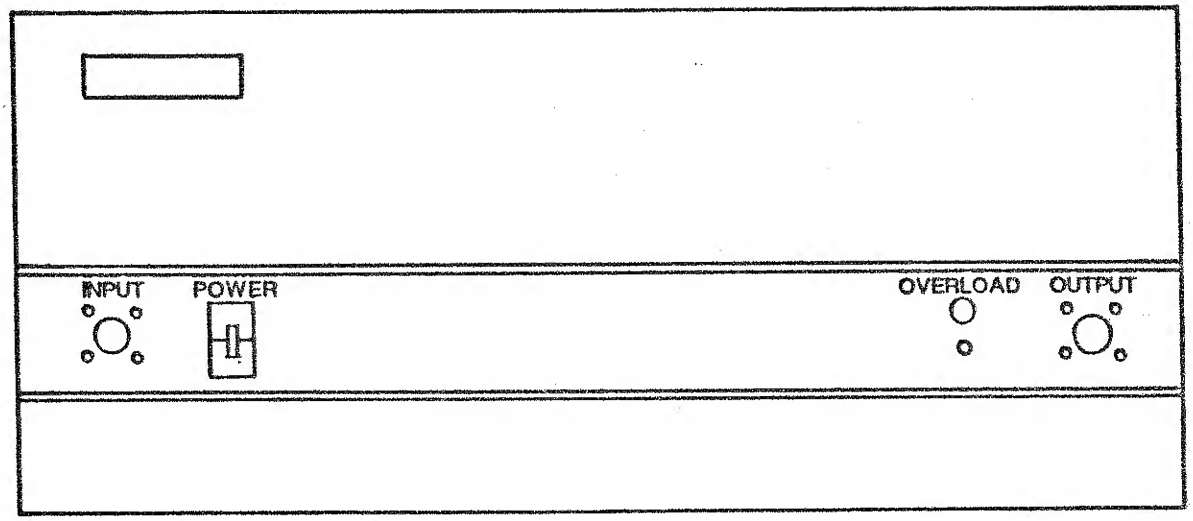

FIGURE 2.1

AMPLIFIER OPERATION

Turn On Sequence:

1. Connect input signal to INPUT connector.
2. Connect load to OUTPUT connector.
3. Select either 120/240 VAC operation by means of switch located on rear of unit.
4. Activate power switch to ON position. A red indicator light mounted within the switch will light when power is applied.

CAUTION:
DO NOT CONNECT UNIT TO 240 VAC MEASURED LINE TO LINE. TO DO SO WOULD RESULT IN ONE SIDE OF THE LINE NOT BEING FUSED, CREATING A HAZARDOUS SITUATION. THE 240 VAC FEATURE IS DESIGNED PRIMARILY FOR USE IN COUNTRIES HAVING 240 VAC MEASURED LINE TO NEUTRAL.

SECTION III

THEORY OF OPERATION

3.1 INTRODUCTION

Refer to Block Diagram No. 1001676.

The input signal to the amplifier is connected through directional coupler (A3A4) and gain equalizer (A3A5) to J1 of low level/driver amplifier (A1). A1 consists of low level amplifier (A1A1) and driver amplifier (A1A2). The gain of A1 is 36dB minimum.

The output of A1 drives the input of final amplifier (A2), where the input signal is split by A2A5 into four equal signals and drives power amplifiers A2A1, A2A2, A2A3 and A2A4. Their outputs are combined together by power combiner A2A6 and drives the 10 watt RF output. The gain of final amplifier A2 is 4dB minimum.

The low level/driver Amplifier A1 consists essentially of five (5) cascaded stages of broadband transistor amplifiers and a two stage output which yield a total power gain greater than 36dB. Input and output matching networks are utilized to provide optimum power transfer of the signal to and from the amplifier with a 50 ohm source and load impedance. Intra-stage feedback is also used to further flatten the frequency response and bias stabilization of the individual stages is provided.

The self-contained power supply employs a full wave rectifier, two (2) integrated circuit regulators to provide stable, low ripple, regulated output voltages.

3.2 AMPLIFIER SECTION

The Model 10W1000 contains a low level driver amplifier and a final amplifier. Each will be explained.

3.2.1 Low Level Driver Amplifier

Refer to Schematic Diagrams No. 1001676, 1002044, and 1001495.

The low level driver amplifier is shown in block diagram No. 1001676.

The input signal to the amplifier is fed from the input connector through a matching network to the base of the first transistor amplifier stage. The component values in this network are chosen to effect a compromise between obtaining the best VSWR and the lowest insertion loss.

The first stage is connected in the common emitter mode with the emitter connected to ground through two resistors. This configuration allows the selection of the emitter resistors to achieve the desired stage gain. The collector voltage (+) is supplied to this stage from the transistor immediately above it (refer to Diagram No. 1001495). This allows the RF transistor to operate at a constant DC current and provides a high degree of protection since the transistor current is independent of overdrive and/or short circuits. Temperature dependence is also avoided. The required decoupling and bypassing of the positive supply is provided by ferrite beads and capacitors.

A coupling network is used to route the output of the first stage to the base of the second stage. The first five stages are coupled in substantially the same manner with the fifth stage matched to a 50 ohm output impedance.

The output of the fifth stage (refer to Diagram No. 1002044) is applied through an input matching network to the input of the 2 stage output amplifier, Q2. The collectors are transformer coupled to the output, which has a 50 ohm impedance. Q1 and Q3 are bias stages for Q2 and help Q2 to operate at a constant DC current.

3.2.2 Final Amplifier

Refer to Schematic Diagrams No. 1001676 and 1001678.

The final amplifier is shown in block diagram No. 1001676. The input signal is split by A2A5 into four equal signals and drives four identical power amplifiers. Only one will be discussed.

The input signal is applied through an input matching network to the input of the 2 stage amplifier Q2.

The collectors are transformer coupled to the output which has a 50 ohm impedance. Q1 and Q3 are bias stages and help to operate Q2 at a constant bias.

3.3 POWER SUPPLY SECTION

Refer to Schematic Diagrams No. 1001208.

Input AC power is fed through RF1 filter FL1 before being switched by the main power switch, S1. The AC power indicator is an integral part of S1. S2 serves to select the primary tap configuration of T1 for operation on either 120 or 240 VAC.

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The power supply utilizes a full wave rectifier on A1 and A3 assemblies. DC output from the rectifiers is filtered by C1. A1 supplies regulated +VDC to the low level amplifier (A1A1) and A3 supplies regulated +VDC to the driver amplifier (A1A2). A1 supplies +VDC to the protection circuit assembly, A2.

3.3.1 Regulators MPLV

3.3.1.1 Regulator A3A3

Refer to Schematic Diagram No. 1001098.

The full wave rectifier consists of CR1 and CR2. Capacitors C1 and C2 are connected in parallel across the rectifiers to suppress transients caused by the reverse recovery of the diodes. The filtered DC output from the rectifiers pass through the series regulator U1, pre-regulator and current boost transistor located external to regulator assembly. U1 is a linear integrated circuit with adjustable output current and voltage. R2 adjusts the output current and R3 adjusts the output voltage. U1 also contains power limiting, thermal shutdown and input overvoltage protection.

The overload light DS2 is located on the front panel and will light when regulated VDC approaches zero. A crowbar will cause DS2 to light and must be reset to restore proper operation. To reset the crowbar reduce the input to 0dBm and push the red switch (S3) located under the overload light on the front panel.

3.3.1.2 Regulator A3A1

Refer to Schematic Diagram No. 1001507.

The full wave rectifier consists of CR1 and CR2. Capacitors C1 and C2 are connected in parallel across the rectifiers to suppress transients caused by the reverse recovery of the diodes. The filtered DC output from the rectifiers pass through the series regulator U1. U1 is a linear integrated circuit with adjustable output current and voltage. R2 adjusts the output current and R3 adjusts the output voltage. U1 also contains power limiting, thermal shutdown and input overvoltage protection.

R1 and VR1 output voltage goes to DS2 and protection circuit.

3.3.2 Protection Circuit

Refer to Schematic Diagram No. 1001132.

The Protection Circuit consists of a DC amplifier U1 with its bias circuit, an SCR crowbar Q2, and optical coupler U2. The input signal at E2 originates from a peak detector which detects the RF input level and delivers an equivalent DC potential to the DC amplifier. The input signal is amplified to the desired level. R15 adjusts the threshold setting which turns ON Q2. With Q2 turned ON, the +28VDC at E5 is pulled close to ground and the A1 regulator output is near zero thus removing the DC power to the driver amplifier (A1A1). Holding current is supplied to E1 from the A1 regulator, through R8 and CR2 and Q2 anode. Thus when Q2 turns ON, it stays ON until the RF amplifier is reset. To reset, reduce the input RF to 0dBm and push the red switch (S3) located on the front panel.

The Optical Coupler U2 is used to sense when any Driver or Final regulator output voltage has decreased below a preset value. Should this happen, the output of the Optical Coupler will turn Q2 ON and cause the RF to the Driver and Final amplifiers to turn OFF, thus protecting the output circuits. The red overload light on the front panel will light. To reset, reduce the input to 0dBm and push S3 located on the front panel.